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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,690	05/22/2004	Fernando Gallego Hugas	8160ES	3689

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EXAMINER	
HAILU, KIBROM T	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,690	GALLEGO HUGAS ET AL.	
	Examiner	Art Unit	
	Kibrom T. Hailu	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are objected to because of the following informalities: Any limitation(s) within parentheses such as "1, 2, 3, 4", "10, 20, 30, 30", "START", "SYNC", "according to the number of slave devices present in the system" in claims 1 and 2 and so on are not considered. Applicant is advised to either cancel the limitations within the parentheses or take out from the parentheses. It is also unnecessary to put numbers in the claims while they are clearly shown in the specification or drawings. They create confusion with the citations that would be given from prior art references.

Claim 6 recites the limitation "packet (10, 20, 30, 40)" in line 3. It is assumed packets P1, P2, P3, P4.

The limitation "slave devices" and "slave circuits" are inconsistently used in the claims, e.g. see claims 1.Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "said short time interval" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "...by the same" in line 6. It is unclear what is claimed. For the purpose further examination, it is considered as "....by the slave devices"

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-3, 5-6, 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris (US 4,937,811) in view of Hansen (WO 94/26558).

Regarding claim 1, Harris discloses a distributed system for acquiring remote data in packets with a communication protocol optimizing the transmission speed (Figs. 6, 7 and 8), particularly applicable to the follow-up and control in an automotive vehicle of the values of signals provided by a series of transducer devices (1, 2, 3, 4) distributed in different parts of the vehicle and which follow different analog or digital values (Fig. 8; col. 3, lines 19-25; col. 7, lines 53-59, 64-66; col. 4, lines 7-13, explaining the messages or signals are associated with sensors or components of the automobile, such as switchs, lamps motors, consoles, control doors, control trunk functions and so on), characterized in that said transducer devices (1, 2, 3, 4) are associated to respective slave/subordinate circuits (10, 20, 30, 40) which are connected, through

a single, time-shared serial communications bus (60), to a master/main circuit (50) (Figs. 6 and 8; col. 7, lines 6-7; 52-59, illustrate slaves are coupled to a master control via a communication network such as 113, and the slaves are associated to components of the automobile), which in turn is connected to a digital processing unit (DP) through a parallel bus (70) (Figs. 6 and 8; col. 7, lines 7-9, 50-52, explain the system microprocessor, such as 110 and/or 150, is coupled to the master controller via the parallel interface buses or links), each one of said slave circuits (10, 20, 30, 40) and master circuit (50) being provided with a respective digital processor (SLV1, SLV2, SLV3, SLV4, MST) and a respective transceiver device (11, 21, 31, 41, 51) (Figs. 1, 2, 3 and 8; col. 3, lines 41-50; col. 3, line 65-col. 4, line 16; col. 7, lines 36-38, the master line interface module such as 10 and slave line interface module 40 include controllers or processors, transmitters and receivers), and which master circuit (50) is provided so as to perform, upon petition of an activation by said unit (DP), a repetitive or non-repetitive consultation, setting up communication with each one of the slave/subordinate circuits (10, 20, 30, 40) according to a communication protocol without error correction which includes a series of bit packets (P1, P2, P3, P4) (Figs. 6 and 8; col. 7, lines 50-53; col. 5, lines 6-9, lines 60-63, explains the microprocessor is communicated through the master controller. It is also obvious for processor to control, order and/or consult the devices such as the master and slaves to with each other), lines , each one of which comprises: a start bit (START) with a longer duration/length than the data bits so that it is fully identified (Fig. 5; col. 5, lines 63-68, the start bit and the P/C bit can be considerd as one (START) because the P/C identifies the message type same as the applicant points it out, thus longer (twice) in duration. Note that the duration of bit type can be changed based on the clocks, and is a design chiose); one or more (according to the number of slave

devices present in the system) address bits (A1, A0), indicative of the slave/subordinate device (10, 20, 30, 40) to be consulted (Fig. 5; col. 5, line 68-col. 6, line 1); and

several data bits (D0...Dn) containing information coming from the consulted slave device (10, 20, 30, 40) (Fig. 5; col. 6, lines 1-2).

Harris doesn't 1.5 delay/synchronism bits (SYNC) for the frames going from master to slave.

Hansen teaches sync bits for the packet going from master to slave (see Figs. 5a and 6a, as explained above, the duration of the sync bits can be changed. As can be shown from the figs. The sync bits is twice than the data bits. However it can be easily changed to 1.5 by chaning the duration of the clock or the pulse of the specified bit type(s)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include sync bits into a frame as taught by Hansen, and incorporate it into the frame format of Harris inorder to settle and/or act as a time in which the system as a whole to synchronise, read for another command fransmission/reply.

Regarding claims 2 and 3, Harris discloses said start bit (START) of each bit packet (P1, P2, P3, P4), with a longer duration/length ,at least two times, than the data bits each of the packets, is provided so as to generate a reinitialization of all the slave circuits (10, 20, 30, 40) (Fig. 5; col. 5, lines 63-68, the start bit and the P/C bit can be considerd as one (START) because the P/C identifies the message type same as the applicant points it out, thus longer (twice) in duration. Note that the duration of bit type can be changed based on the clocks, and is a design choise).

Regarding claims 5 and 6, Harris discloses each bit packet(P1, P2, P3, P4) includes an additional last protocol error detection bit (DET) in the data field or address field (Fig. 5, col. 6, lines 2-4, each of the frames such as the one shown in fig. 5 include error detection or CRC. A stop bit is included as a last bit, however it is obvious to put the error detection bit as the last bit and the receiver know it is the last bit).

Regarding claims 8 and 9, Harris discloses said serial bus (60) is formed by a twisted differential cable comprising two twisted or single insulated copper conductor(s) (61, 62) in shunt with a ground line (64) (col. 2, lines 9-12; col. 4, lines 31-36, explains in order to cancel interferences a pair of twisted pair of communication network or bus 113 is used. It would also obvious and well known to use a single copper conductor wire shunt with ground line).

Regarding claim 10, Harris discloses each one of those transducer devices (1, 2, 3, 4) providing an analog signal is associated to an A/D converter (12, 22, 32, 42) connected to the corresponding slave-transceiver circuit (SLV1-11, SLV2-21, SLV3-31, SLV4-41) (col. 6, lines 29-38).

Regarding claim 12, Harris discloses each bit packet (P1, P2, P3, P4) contains, in addition to said one or more address bits (A1, A0), data bits (10-ln) susceptible to being transmitted from the master circuit (50) to the consulted slave circuit (10, 20, 30, 40), such that they are univocally recognized by the same (Fig. 5; col. 5, line 68-col. 6, line 1, it clearly shows the address bits are more than two bits such that the slaves would identify the message.

Regarding claim 13, the claimed process includes the same features as the rejected claim 1 except now the interruption signal that indicate the end of consultation order is sent from the master to the processor while still the master communicates with the slaves. Hansen suggests the

system can work using an interruption function but that is considered to be expensive (page 13, lines 9-16). And it obvious for a system to perform multiple functions through a multi-task processor. That is, it is obvious for the master to send inturrupt instruction or signal while communicating with the slaves to increase the communication speed of the system.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harris in view of Hansen as applied to claim 1above, and further in view of Wang (US 6,507,158 B1).

Regarding claim 4, Harris discloses each bit of the packet has address, data or error detection functions (see Fig. 5, "ADDR" and "CRC"). However, Harris doesn't discloses each of the bits is encoded in Manchester format.

Wang teaches each of the bits is encoded in Manchester format (col. 2, lines 7-23, explains each of the bits such as the START, address, and error detection bits are encoded using Manchester coding scheme).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Manchester coding scheme, known as bi-phase coding, to encode each of the bit types as taught by Wang into the communication system of Harris so that high bit rate operation can be accomplished.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harris in view of Hansen as applied to claim 1above, and further in view of Momona (US 5,440,555).

Regarding claim 7, Harris discloses messages or packets from/to the slave/master devices. However, Harris doesn't explicitly disclose a short time interval (t1) of separation between bit packets (P1, P2, P3, P4) circulating through the serial bus (60) is comprised within a range of 0 to 1 bit.

Momona teaches said short time interval (t1) (guard time) of separation between bit packets (P1, P2, P3, P4) circulating through the serial bus (60) is comprised within a range of 0 to 1 bit (col. 4, lines 30-34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the guard time of non-transmission bit (which is a time within a range of 0 to 1 bit) as taught by Momona between the message formats of Harris so that an overlap of the messages or the frames tramsmitted from the different slaves would be prevented.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harris in view of Hansen as applied to claim 1above, and further in view of Enders et al. (US 6,805,375 B2).

Regarding claim 11, Harris discloses a digital processing unit or microprocessor (Figs. 6 and 8, 110 or 150). However Harris doesn't disclose said digital processing unit (DP) is linked to another bus of the vehicle, such as a CAN or other type of bus.

Enders teaches said digital processing unit (DP) is linked to another bus of the vehicle, such as a CAN or other type of bus (Figs. 1 and 4; col. 3, lines 9-12; col. 5, lines 31-32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to link the processor to another part of the vehicle using CAN as taught by Enders for significant weight savings, reliability, ease of manufacture, and increased options for on-board diagnostics.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harris in view of Hansen as applied to claim 13 above, and further in view of Go et al. (US 5,305,355).

Regarding claim 14, Harris discloses communication between master control or circuit and slave circuits, and the communication is contolled or imposed by the microprocessor.

However, Harris doesn't disclose said consultation cycles between master circuit (50) and slave circuits (10, 20, 30, 40) and acquisition of data stored in the master circuit (50) from the digital processing unit (DP) are carried out cyclically at a predetermined frequency.

Go teaches the consultation cycles between master circuit (50) and slave circuits (10, 20, 30, 40) and acquisition of data stored in the master circuit (50) from the digital processing unit (DP) are carried out cyclically at a predetermined frequency (col. 12, lines 52-56; col. 13, lines 1-3; col. 23, lines 4-12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the process of communication between the master and the slaves at a predetermined frequency or period of time as taught by Go into the communication of Harris so that the respective communications would be consistent and reliable.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harris in view of Hansen as applied to claim 13 above, and further in view of Bottomley (US 6,931,050 B1).

Regarding claim 15, Harris discloses messages having error detection or CRC bits. Harris doesn't explicitly disclose those bit packets (P1, P2, P3, P4) whose transmission has been detected as erroneous by means of said error detection bit (DET) are skipped over, passing to the next bit packets (P1, P2, P3, P4).

Bottomley bit packets (P1, P2, P3, P4) whose transmission has been detected as erroneous by means of said error detection bit (DET) are skipped over, passing to the next bit packets (P1, P2, P3, P4) (col. 8, lines 39-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to skip over the bit frames when the error detection bit or scheme indicates

errors, and use the process into the communication network or protocol of Harris, this way the data communication would be fast, more efficient, and reliable.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom T. Hailu whose telephone number is (571)270-1209. The examiner can normally be reached on Monday-Thursday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

kth
08/03/07

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER